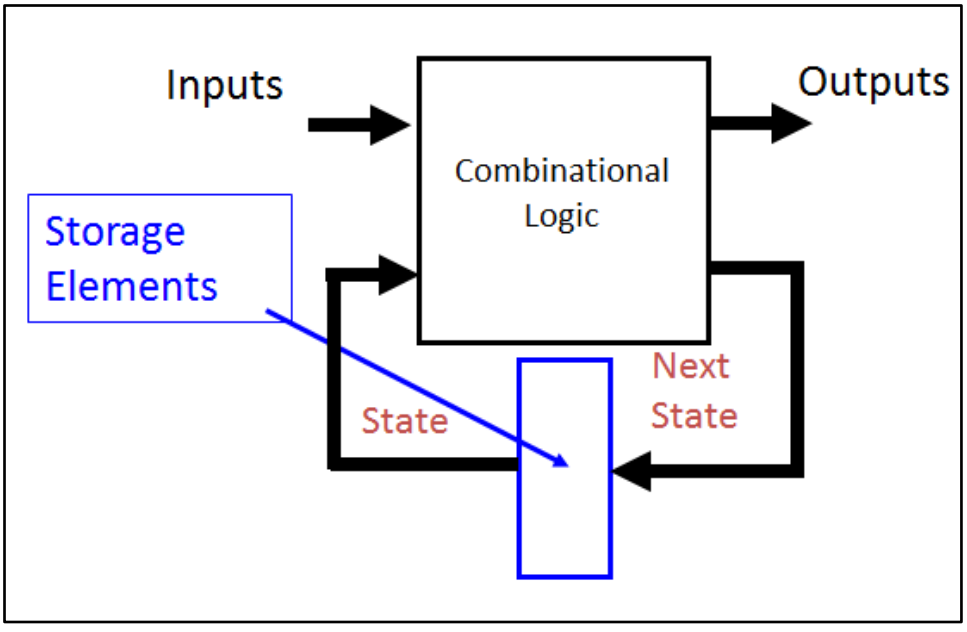
Lecture – 10 - Chapter 5

Outline

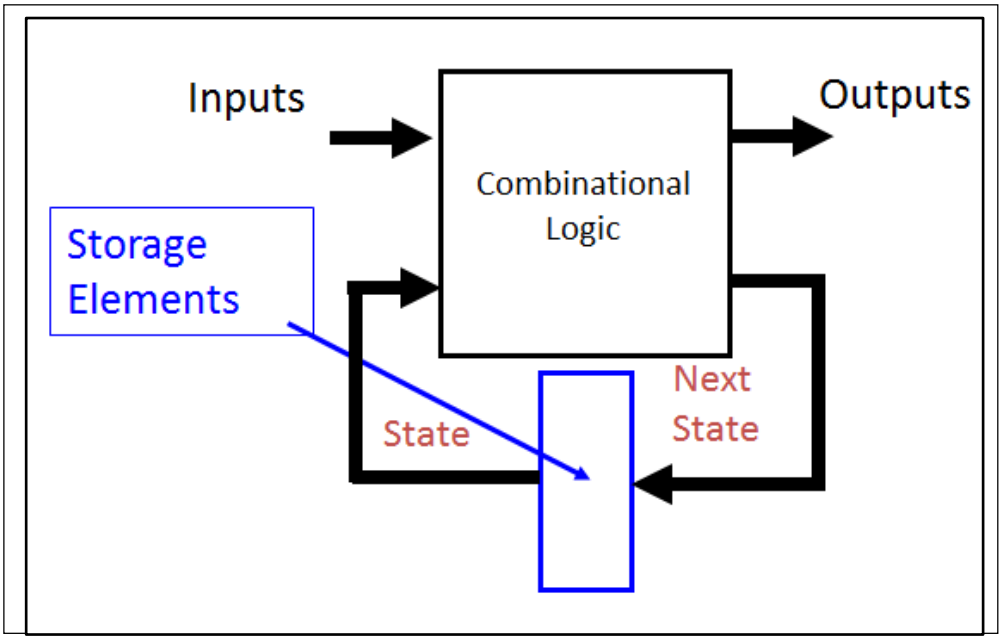
- Introduction to sequential circuits
- Types of sequential circuits
- Storage elements
  - ***Flip-flops***

Introduction to Sequential Circuits

- A Sequential circuit contains:
  - Storage elements:
    Latches or Flip-Flops
  - Combinational Logic:
    - **Implements a multiple-output switching function**
    - Signals from the outside are **inputs.**
    - Signals to the outside are **outputs.**
    - **Other inputs,** State or Present State, are signals from storage elements.
    - **The remaining outputs, Next State are inputs to storage elements.**



- Combinatorial Logic



- *Next state function*
  Next State = f(Inputs, State)

- *Output is a function of inputs and State.*

Types of Sequential Circuits

- Depends on the times at which:
    - storage elements observe their inputs, and
    - storage elements change their state

- Synchronous
    - Behavior defined from knowledge of its signals at discrete instances of time
    - Storage elements observe inputs and can change state only in relation to a timing signal (clock pulses from a clock)
- Asynchronous
    - Behavio
    - r defined from knowledge of inputs an any instant of time and the order in continuous time in which inputs change

    - Nevertheless, the synchronous abstraction makes complex designs tractable!

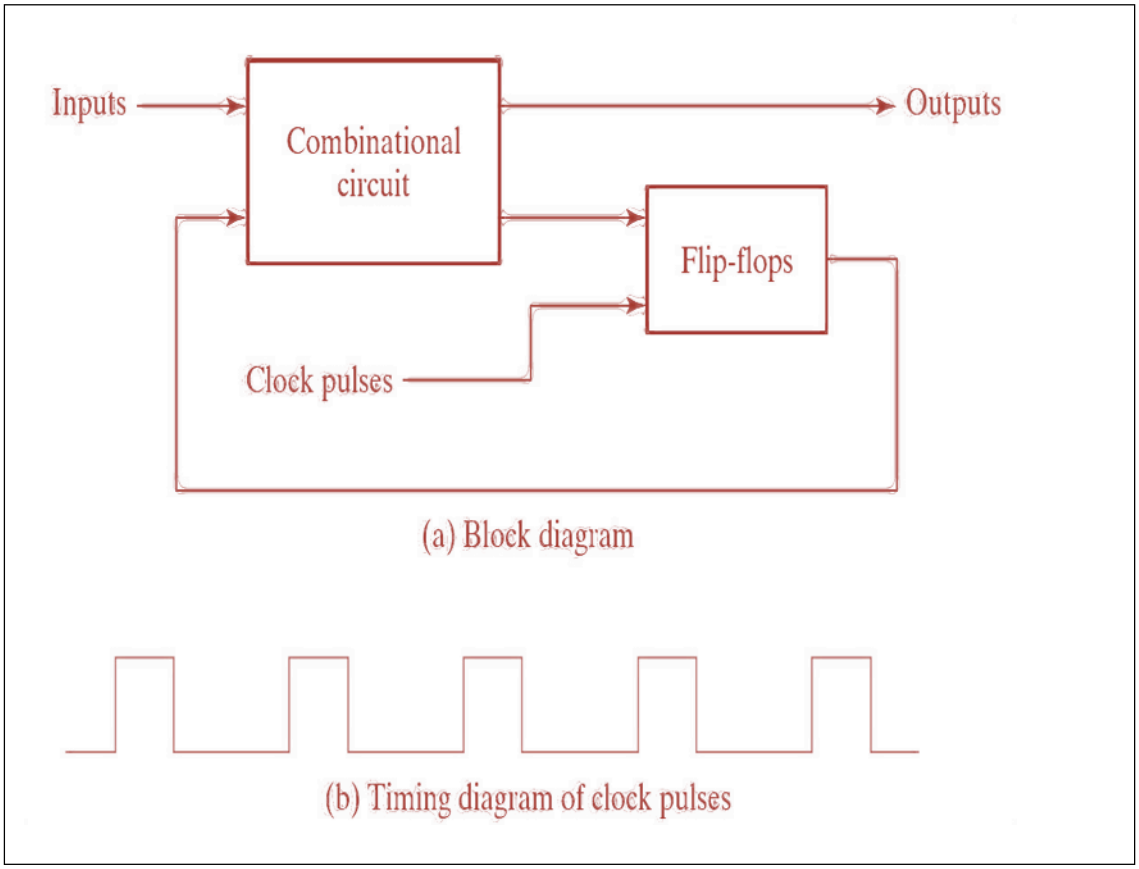
Storage element

- **Storage elements:** devices capable of storing binary information

  flip-flop: used in clocked sequential circuit, storing one bit of information: state

  The flip-flop is updated when a pulse of the clock signal occurs.

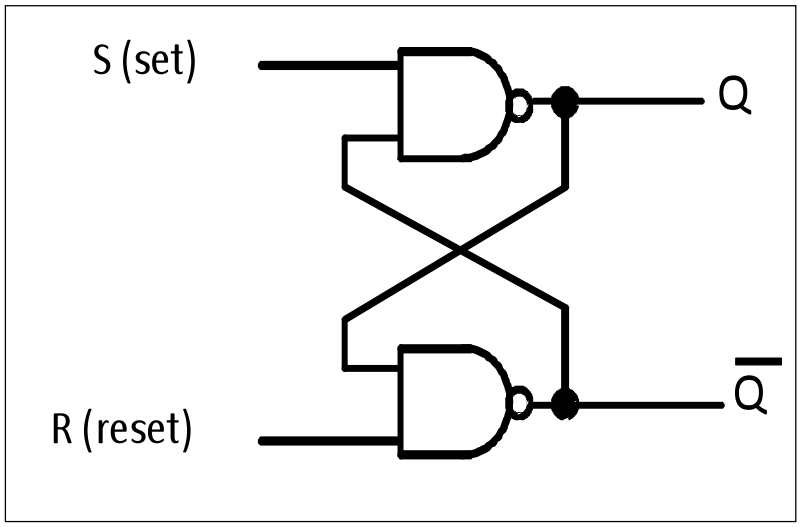
  Latch: basic component of flip-flop.



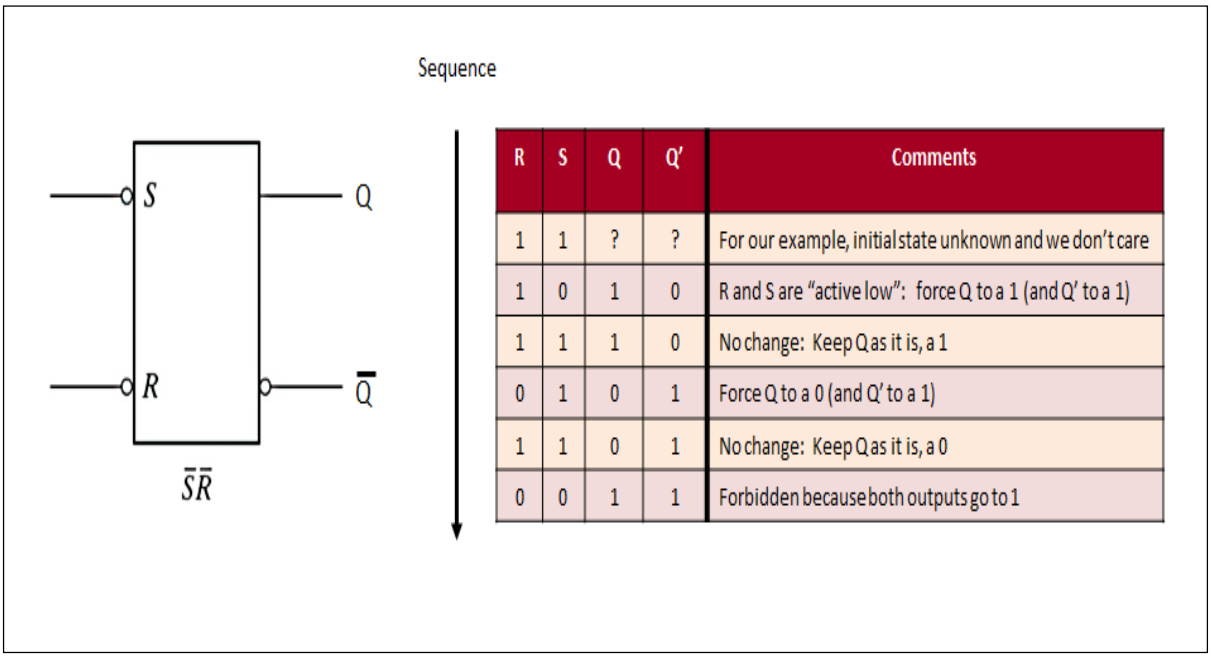
Basic (NAND) S – R (Set-Reset latch)Latch

- "Cross-Coupling" two NAND gates gives the S' -R' (Set – Reset) Latch:

  Which has the time sequence behavior:



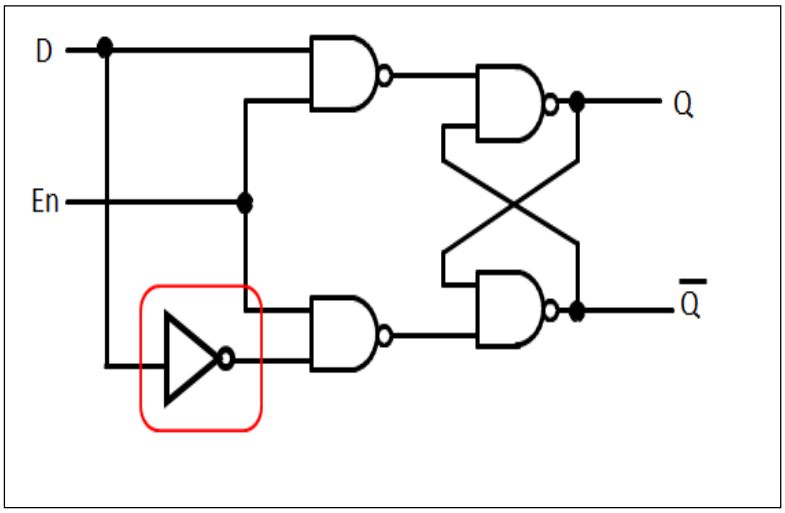
S = 0, R = 0 is <u>forbidden</u> as input pattern



R	S	Q	Q'	Comments
1	1	?	?	For our example, initial state unknown and we don't care
1	0	1	0	R and S are "active low": force Q to a 1 (and Q' to a 1)
1	1	1	0	No change: Keep Q as it is, a 1
0	1	0	1	Force Q to a 0 (and Q' to a 1)
1	1	0	1	No change: Keep Q as it is, a 0
0	0	1	1	Forbidden because both outputs go to 1

D Latch

- Adding an inverter to the S-R Latch, gives the D Latch

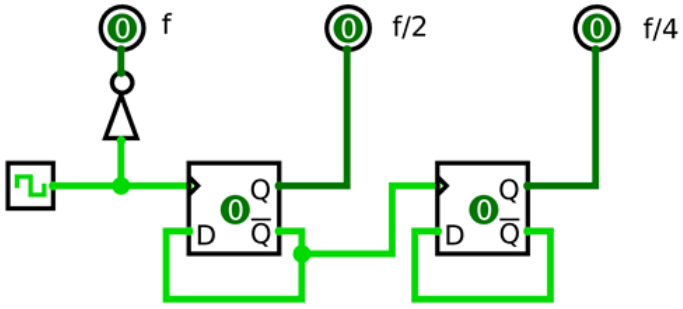


(shown with an enable input)

The enable input often acts as the clock.

- Note that there are no "indeterminate" states!

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state



Flip-Flops

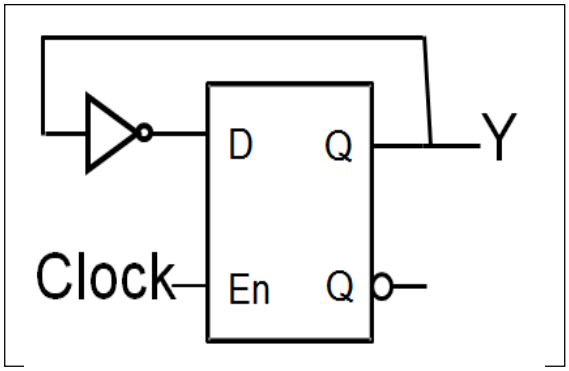
- The latch timing problem
- Edge-triggered flip-flop
- Direct inputs to flip-flops

The Latch Timing Problem

- In a sequential circuit, paths may exist through combinational logic:
  - From one storage element to another
  - From a storage element back to the same storage Element
- The combinational logic between a latch output and a latch input may be as simple as an interconnect
- For a D-latch, the output Q depends on the input D whenever the control input En has value 1

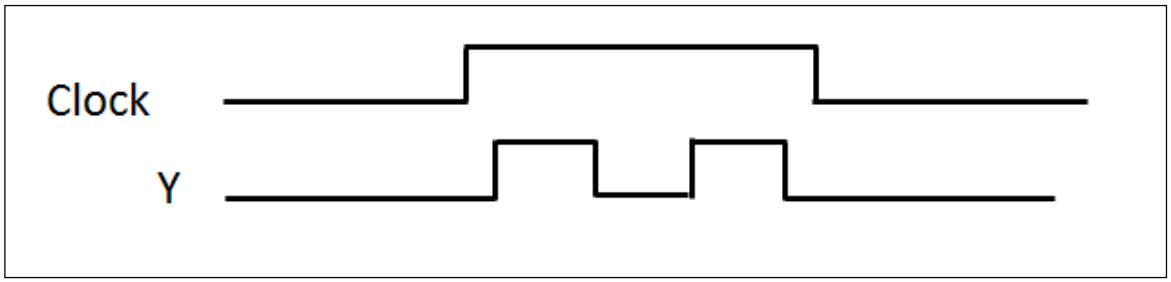
The Latch Timing Problem

- Consider the following circuit:



- Suppose that initially Y = 0.

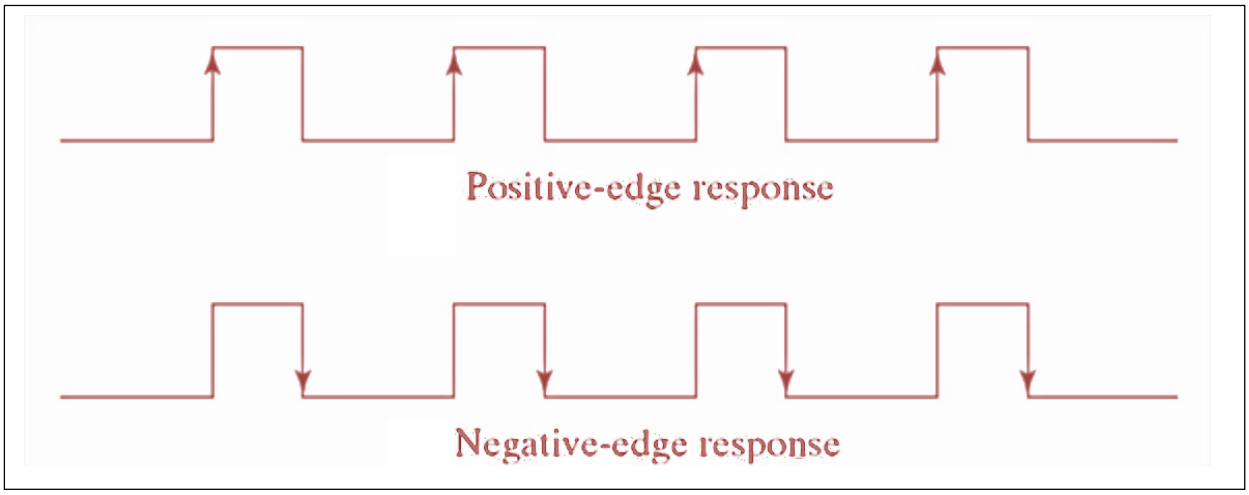
En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state



- As long as En = 1, the value of Y continues to change!
- The changes are based on the delay present on the loop through the connection from Y back to Y.
- This behavior is clearly unacceptable.
- Desired behavior: Y changes only once per clock pulse

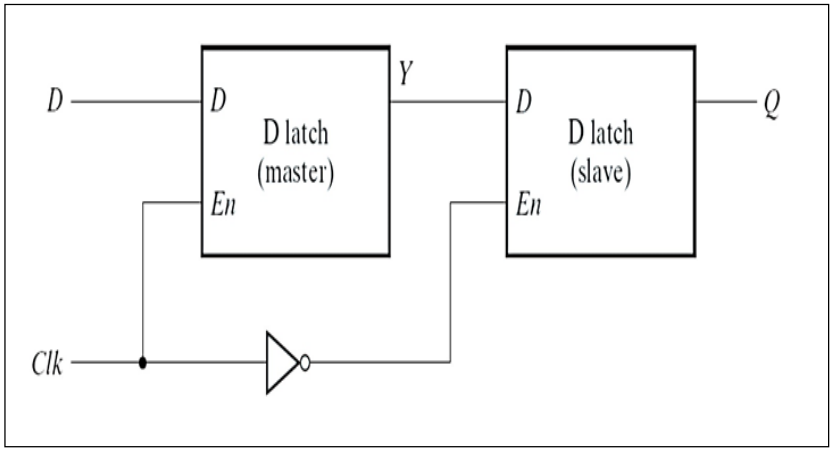
Flip-Flop Solution

- An *edge-triggered* flip-flop ignores the pulse while it is at a constant level and triggers only during a transition of the clock signal
- Edge-triggered flip-flops can be built directly at the electronic circuit level

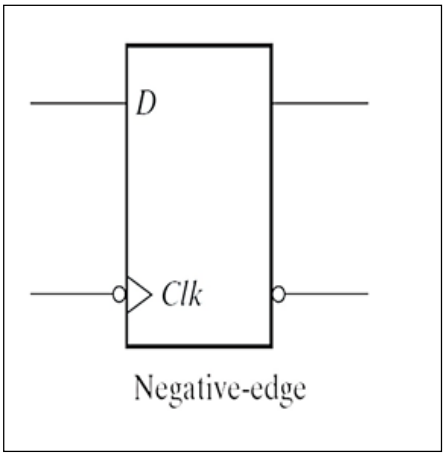


Edge-Triggered D Flip-Flop

- The edge-triggered D flip-flop is the master-slave D flip-flop



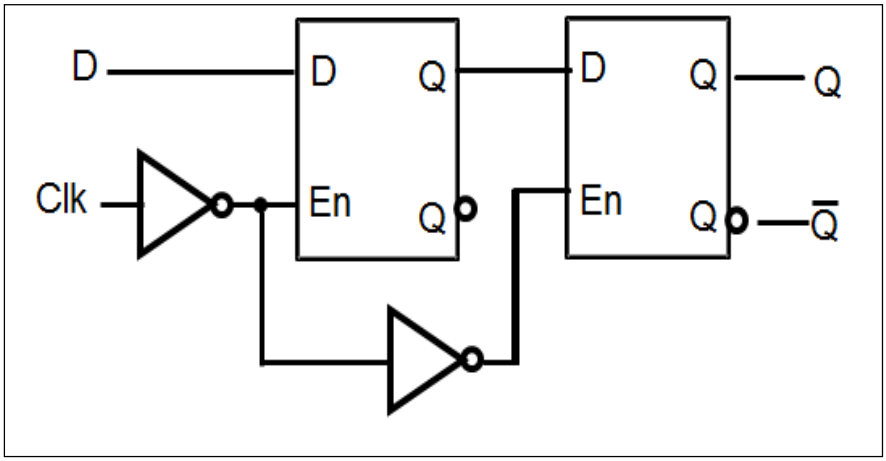
- The change of the D flip-flop output is associated with the negative edge at the end of the pulse



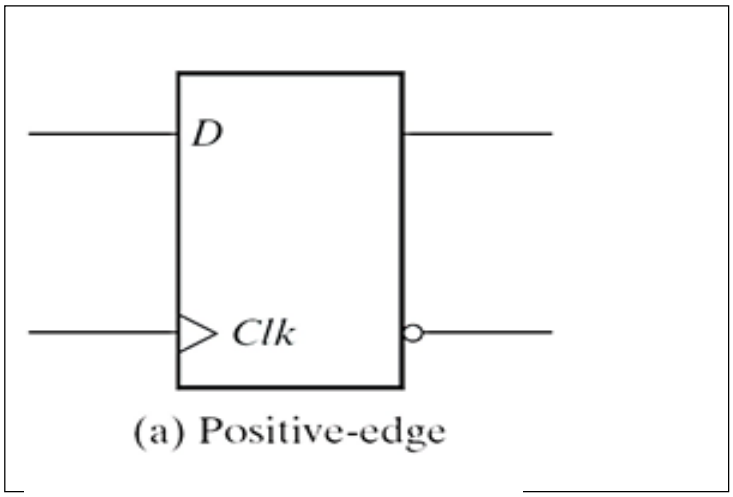
- It is called a ***negative-edge triggered*** flip-flop

Positive-Edge Triggered D Flip-Flop

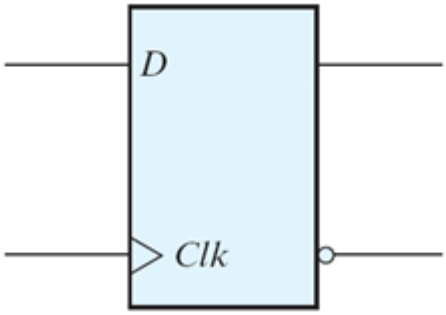
- Formed by adding inverter to clock input



- Q changes to the value on D applied at the positive clock edge within timing constraints to be specified

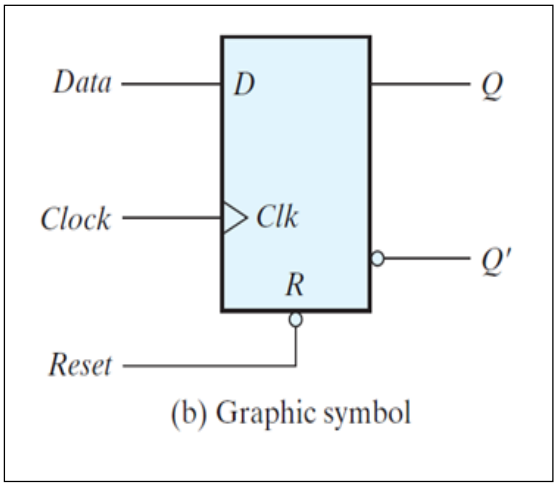


- Our choice as the standar uential circuits



Direct Inputs

- At power up or at reset, all or partof a sequential circuit usually is initialized to a known state before it begins operation



(b) Graphic symbol

- This initialization is often done outside of the clocked behavior of the circuit, i.e., asynchronously.

- Direct R inputs that control the state of the latches within the flip-flops are used for this initialization.
- For the example flip-flop shown
  - 0 applied to R resets the flip-flop to the 0 state

R	*Clk*	*D*	*Q*	*Q'*
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table